OKI *Open up your dreams*

**XILINX®** | ALLIANCE PROGRAM PREMIER MEMBER

Giga bit Ethernet TCP/IP solution for Xilinx FPGA

Xilinx Tri-Mode EMAC supported

Gigabit Ethernet full bandwidth (1.0Gbps) TCP data transfer achieved on FPGA single chip, with TCP/IP protocol stack and TCP offloading engine implemented within Xilinx FPGA. High-speed, highly reliable data transfer achievable.

IPv6 READY

Features
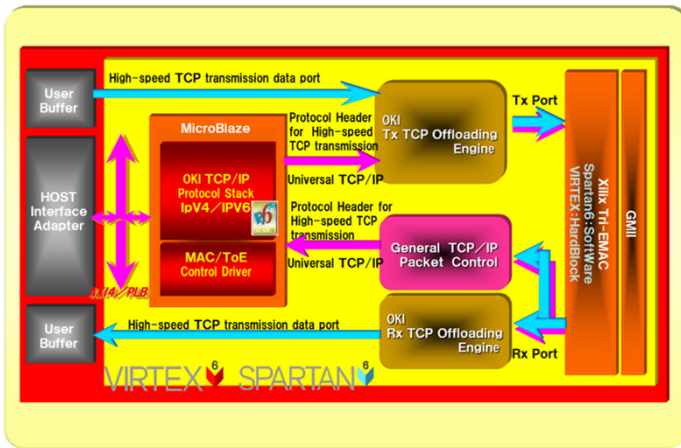
➤ **ToE (TCP Offloading Engine) enables data transfer making maximum use of Gigabit Ethernet bandwidth**

➤ **TCP/IP full stack enables compatibility with various Ethernet protocols.**

➤ **High speed TCP by ToE and universal LAN communication by TCP/IP protocol stack achieved on FPGA single chip.**

★**Multi-session communication supported**

High-Speed TCP Transfer （900Mbps/Gb Ether）

920Mbps

**Cat 6 universal LAN cable (up to 100m direct connect)**

Example of Single Core configuration

SPARTAN 6
VIRTEX 6
KINTEX 7
VIRTEX 7
ARTIX 7
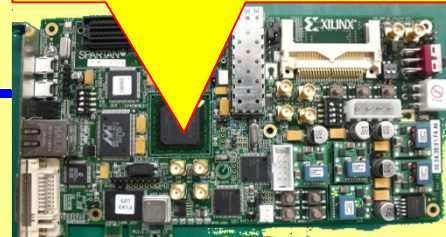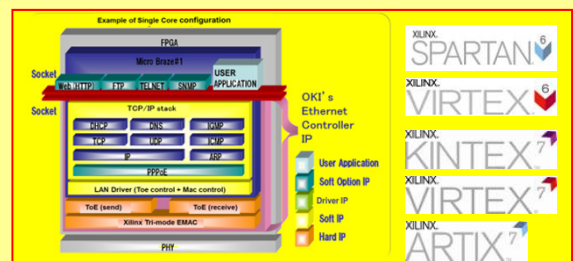
Xilinx FPGA Evaluation Board

Ethernet protocol control is processed within FPGA （Micro Braze™）

Hardware engine （ToE） + TCP/IP protocol stack achieves high-speed data transfer!

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●Giga bit Ethernet TCP/IP Full Protocol Stack IP Core Configuration（example）

Example of Single Core configuration
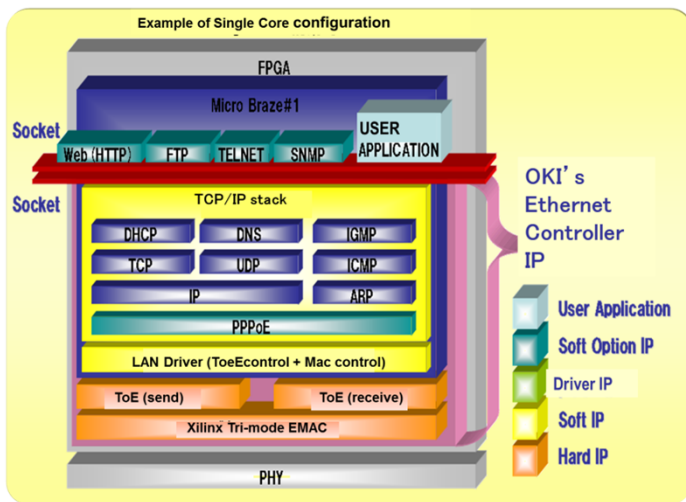
- ➡ **OKI's TCP/IP full stack**, MAC/PHY control driver, and control driver for controlling **TOE (TCP Off Loading Engine) IP** implemented on MichroBlaze software processor, achieving large capacity, high speed TCP transfer.

- ➡ Standard socket interface is used for interfacing to user application and optional software IP. So when application and stack share the same processor, interfacing between software is possible only with standard socket interface.
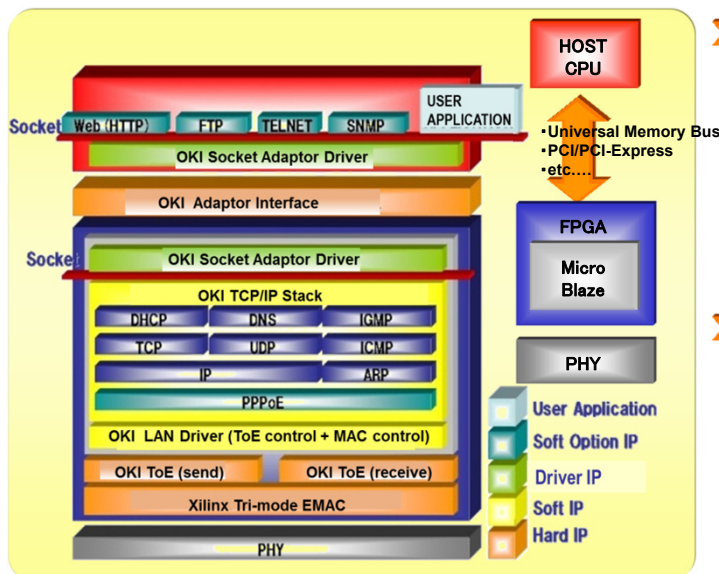
- ➡ In the configuration where application and stack are implemented to different processors, stack and application can be interfaced via socket adapter consisting of software and hardware.

  ※ **Socket adaptor (HW/SW) also available as optional IP, so there is no need to modify application API.**

- ➡ Interface between socket adaptors can be modified to desired interface with customization.

  High performance TCP/IP communication will be possible, just by implementing the IP on FPGA as hardware.

iTOE solution contains

Full development environment required for FPGA designing, including IP, reference design, ISE/EDK project and manuals

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